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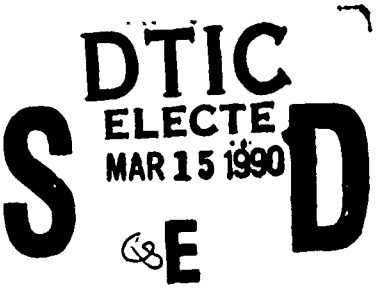

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During the first quarter we began work directed at the Si-GaAs interface formation. This work encompasses the in situ cleaning process and the Si deposition process. Advances have been made in the GaAs in situ cleaning. The reasons for the advances, recognition of SiO_2 deposition byproduct residue and addition of a load lock to the system, are described. Work towards improving the pseudomorphic Si deposition is also described.

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During the second quarter work continued on the GaAs-Si interface formation. We had noted improvements in the low-temperature Si epitaxial deposition through the incorporation of hydrogen in the deposition environment. Also we noted improvements in the Si deposition through the use of lower pressure conditions. The results of the use of MIS results obtained on both p-type and n-type GaAs with partially optimized processing are described. These Si deposition conditions for MIS structure formation are described.

During the third and fourth quarters work again continued on the GaAs-Si interface formation. During this period a series of experiments was performed to evaluate the effects of processing conditions on the p-type GaAs MIS structure.

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1.0 INTRODUCTION

The following report conveys the progress made for first year from July 1, 1988 to June 30, 1989 for ONR contract number Number N-00014-88-C-0433. The program involves investigation of pseudomorphic insulator structures on GaAs.

During the first quarter we began work directed at the Si-GaAs interface formation. This work encompasses the in situ cleaning process and the Si deposition process. Advances have been made in the GaAs in situ cleaning. The reasons for the advances, recognition of SiO_2 deposition byproduct residue and addition of a load lock to the system, are described. Work towards improving the pseudomorphic Si deposition is also described.

During the second quarter work continued on the GaAs-Si interface formation. We had noted improvements in the low temperature Si epitaxial deposition through the incorporation of hydrogen in the deposition environment. Also we noted improvements in the Si deposition through the use of lower pressure conditions. The results of the use of MIS results obtained on both p-type and n-type GaAs wth partially optimized processing are described. These Si deposition conditions for MIS structure formation are described.

During the third and fourth quarters work again continued on the GaAs-Si interface formation. During this period a series of experiments was performed to evaluate the effects of processing conditions on the p-type GaAs MIS structure.

2.0 GaAs SURFACE CLEANING

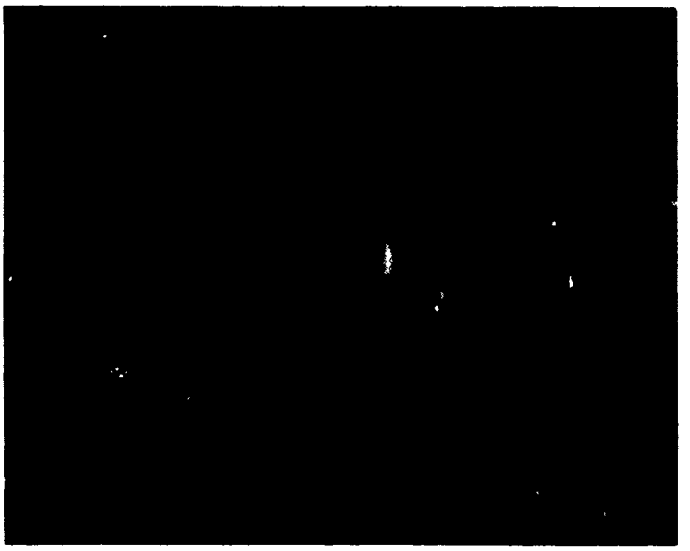
The native oxides of GaAs are very poor electrically. It is imperative that any native oxide be removed from the GaAs surface before depositing the Si-SiO_2 insulator structure. During the in situ cleaning process the environment must be oxygen free to avoid competitive cleaning and oxidation processes. From joint RTI(CSR)-NCSU(Physics) dielectric programs, it has been shown that the SiO_2 deposition process results in formation of OH species (such as H_2O) which contaminate the processing environment. These OH groups are basically removed from the substrate thermally during deposition. Deposits in the chamber walls are formed at relatively low temperatures (25 to 100 ° C), so that the OH groups are heavily incorporated in these deposits. Subsequent plasma assisted processing can release these deposits leading to process contamination. At present the oxide deposition parameter matrix is being examined to alleviate this by-product formation problem. In lieu of an improved oxide deposition process, we have implemented chamber conditioning sequences which reduce the effects of wall deposit contamination sources.

The addition of a vacuum load lock to the system has made the chamber preconditioning possible. The chamber can be conditioned prior to wafer introduction. The wafer can subsequently be introduced into the chamber, in vacuo, avoiding chamber contamination from the outside environment. In fact the addition of the vacuum load lock made us aware of the magnitude of the problem caused by the wall deposits. After oxide processing it is difficult to pump the chamber below the 10^{-6} Torr range without some kind of chamber conditioning (either 250 ° C

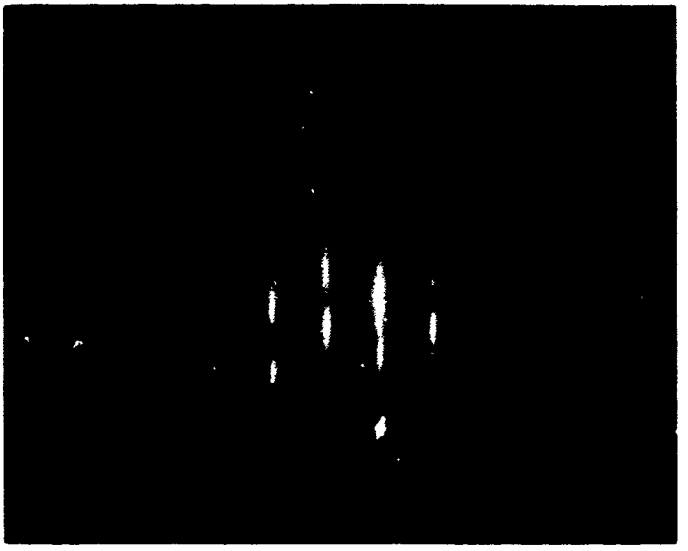
baking for at least 12 hrs. or a noble gas plasma treatment). This outgassing problem is caused by the water, generated during the deposition process, which remains in the chamber after processing. The OH groups incorporated in wall deposits can be released during subsequent plasma processing such that the partial pressure of OH in the chamber can be very high during the processing. This phenomenon has been confirmed by mass spectroscopy.

We have noted improved surface cleaning results following both noble gas plasma scouring of the chamber, and following long Si or Si_3N_4 depositions. The noble gas plasma cleaning process helps get rid of the contamination, while the deposition processes encapsulate the contaminants.

The best result in GaAs cleaning to date as analyzed by RHEED is shown in Figure 2.1.



GaAs Before Hydrogen Treatment



GaAs After Hydrogen Treatment

2.1: GaAs surface after in situ hydrogen clean. Note 4th order reconstruction.

3.0 SILICON INTERLAYER DEPOSITION STUDIES

The benefits of load locked wafer introduction has also had an impact on the Si interlayer studies. The load lock allows us to perform 3 runs a day and to perform chamber conditioning steps between each run. Faster turn-around time is allowing more complete investigation of deposition parameters.

We have begun investigation of the effects of the following processing parameters and processing modifications on the Si epitaxy: deposition temperature, pulsing of the Si deposition, deposition pressure, and addition of H_2 gas to the SiH_4 flow.

Under the present system configuration it is advantageous to perform the in situ cleaning operation and the interlayer deposition at the same temperature. Approximately 5 to 10 minutes is required to raise or lower the temperature 50 ° C. (Any time lag between the in situ cleaning and the deposition is an opportunity for surface contamination or oxidation to occur. Even the time required to perform the RHEED analysis enhances the opportunity for contamination to occur. The ideal sequence is one in which the cleaning, interlayer deposition and insulator deposition are carried out sequentially with no delay between the steps. Modification of the sample heater stage and controller would allow the temperature to be ramped up and down more rapidly. In any case, it is best to degas the heater stage and sample at the highest temperature to be used during the processing to avoid excessive outgassing.

We have begun to investigate the effects of pulsed deposition on film quality. In this process the SiH_4 is turned on for 10 to 20 seconds, then off for 10 to 20

seconds, then back on. During the SiH_4 off period, the Ar plasma remains on. These experiments are being performed on Si substrates to look at the epi quality with no lattice mismatch. Energy imparted by the Ar plasma during the off period may aid in the dehydrogenation of the surface. Experiments thus far indicate that if the off period is too long, the epi quality degrades, probably from contaminant incorporation.

We have also begun investigating the effect of low pressure on epitaxial Si deposition. Experiments conducted thus far indicate that the Si deposition rate is higher at lower pressures particularly at higher SiH_4 flow rates. We have noted an increase of 3 in the deposition rate (2 nm per minute to 6 nm per minute) for a drop in pressure from 0.20 torr to 0.06 torr with 50 sccm of 2% SiH_4 flowing. The data on the Si deposition rates is shown in Table 3.1. The Si deposition rates were determined by depositing the Si on Si substrates coated with pyrolytic Si_3N_4 to serve as a stop etch. Patterns were etched in the deposited Si and the step height measured with an Alpha Step profilometer. Further experiments are underway to determine the effect of deposition rate on the quality of the epitaxial Si.

Preliminary results indicate that the addition of H_2 to the SiH_4 flow improves the quality of the epitaxy. It is possible that the H_2 both increases surface mobility of the Si atoms and helps remove any impurities that may land on the surface during deposition.

TABLE 3.1:

Si Deposition Growth Rate

As a Function of Pressure and Silane Flow Rate

Sample	Flow Rates			Growth Pressure (mbar)	Growth Temperature (°C)	Growth Time (min)	Film Thickness (Å)	Si Deposition Rate (Å/min)
	Plasma Feed (sccm)	Ring Feed (sccm)						
	Ar	SiH_4	Ar					
111688-1	200	5	100	0.0723	300	120	585	4.88
112388-3	200	5	100	0.20	300	90	478	5.31
112288-1†	200	5	100	0.0723	300	120	235	1.96†
112388-1	200	20	100	0.0723	300	30	640	21.30
112388-2	200	20	100	0.20	300	30	380	12.67
112288-3	200	50	100	0.0723	300	15	900	60.00
112288-4	200	50	100	0.20	300	15	305	20.30
112888-1	200	2	100	0.20	300	180	340	1.88
120588-1‡	200	50	100	0.0769	300	30	860	28.67‡

† Pulsed growth (10s on, 10s off) ‡ 50 sccm H_2 through ring-feed

To date, the evidence indicates that the single most important factor for the Si interlayer deposition is to have a clean surface prior to deposition. Any native oxide that remains on the surface will degrade the material. SiO_2 on Si is particularly difficult test case because the SiO_2 is very difficult to completely remove at low temperatures.

4.0 GaAs MIS STRUCTURES USING IMPROVED Si DEPOSITION CONDITIONS

Improvements in low temperature Si epitaxial deposition have been noted with the use of low pressure deposition conditions and with the inclusion of hydrogen in the deposition environment. The improvements have been evidenced by improvements in RHEED characteristics of deposited Si on Si and from TEM analysis of Si on Si structures. These conditions were applied to the GaAs pseudomorphic insulator structure. We found that the addition of the hydrogen to the Si on GaAs deposition process led to severe pinning of the GaAs surface. The capacitance voltage characteristic of GaAs MIS structures using the --hydrogen-silane at low pressure-- deposition parameters showed very little voltage dependence. The maximum value of capacitance for the structures indicated that their surfaces were depleted. Figure 4.1 shows a nominal characteristic from one of these samples. The material is n-type GaAs on n+ substrate material. Removing the hydrogen from the Si deposition parameters led to immediate improvements in the electrical characteristics of the MIS structures as described in the following section. Thus the preliminary conclusion is that the activated hydrogen at low pressure is more efficient at etching and disproportionating the GaAs surface.

4.1 p-Type GaAs MIS Results

The GaAs pseudomorphic insulator structure was applied to a p-type GaAs sample. The GaAs material is a p-type epilayer doped 1×10^{15} cm^{-3} with carbon on a heavily doped p-type substrate. The material was obtained from KOPIN.

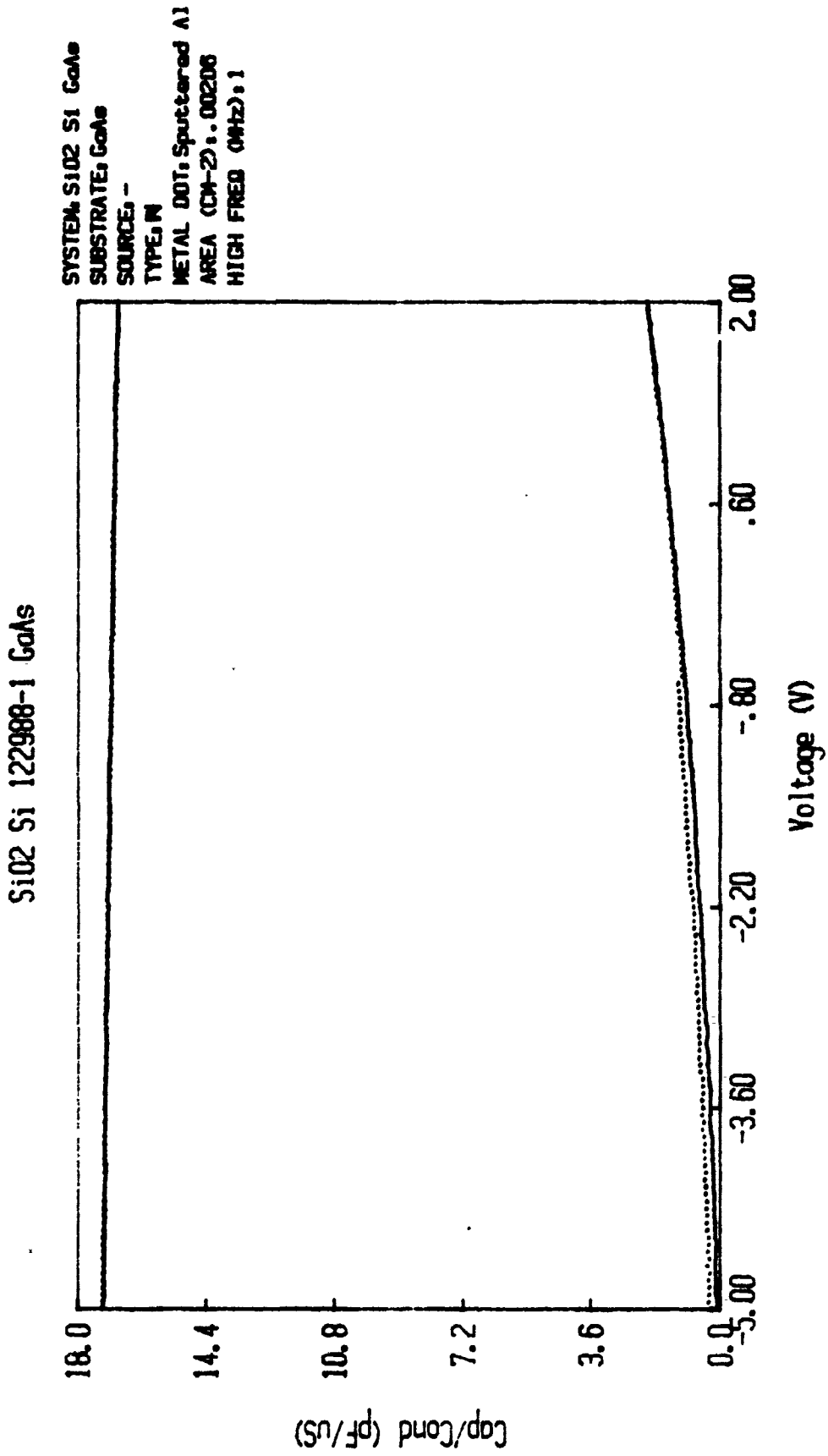


FIGURE 4.1: 1 MHz C/V, G/V data from a pseudomorphic insulator structure in which H_2 was included during the Si deposition. The surface in this case is severely pinned.

The sample was processed as follows:

1. Standard GaAs surface clean--[etch 30 seconds in $NH_4OH(1)-H_2O_2(2)-H_2O(1600)$, stop etch $NH_4OH(1)-H_2O(15)$, blow dry]

2. 10 second activated hydrogen preburn at 0.200 Torr.

3. 1 nm Si deposition at 0.075 Torr.

4. 15 nm SiO_2 deposition at 0.080 Torr.

The characteristics of the MIS capacitors fabricated on this material are shown in Figure 4.2. These structures exhibit only 0.035 V of hysteresis in the high frequency capacitance, compared to 0.7 V for the previously reported structures. The frequency dispersion in the range of zero Hz.(quasistatic) to 10 MHz is also reduced from that of the previous structures. The range of gate bias over which the characteristics occur is -3.5 to 2.0 V which represents a working field range of -2.3 to 1.3 MV/cm. The SiO_2 insulator is certainly capable of sustaining such fields. The details of the origin of the frequency dispersion and the hysteresis are still under investigation.

4.2 n-Type GaAs MIS Results

The n-type GaAs structures were processed in a different manner from the p-type structures. The n type epitaxial material was grown in house by MOCVD and transferred directly into the RPECVD system for formation of the insulator structure. The in situ processing was the same as for the p-type structure. The SiO_2 thickness was 10 nm. There was a slight morphology problem with this material which influenced the yield of the devices. However several devices could be

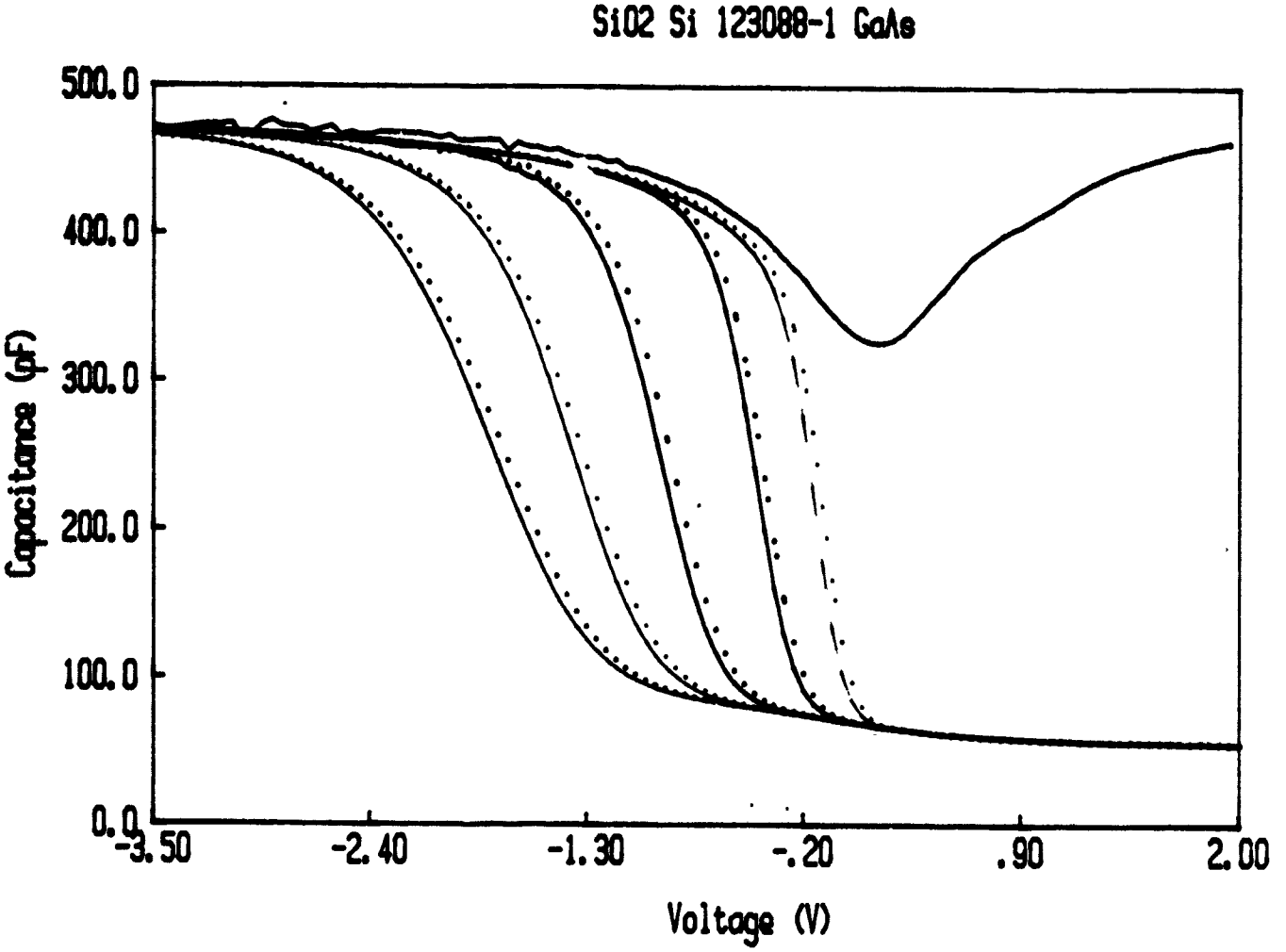


FIGURE 4.2: Multiple frequency C/V data from a p-type GaAs-pseudomorphic insulator MIS structure. The frequencies are (left to right) 10 MHz. 4 MHz. 1 MHz. 100 KHz, 10 KHz. and quasistatic.

characterized. The characteristics are shown in Figure 4.3. Again note the reduced level of hysteresis. The quasistatic characteristic shows a deep depletion type characteristic which is indicative of a low minority carrier generation rate i.e. long lifetime. Further analysis of the device characteristics is underway.

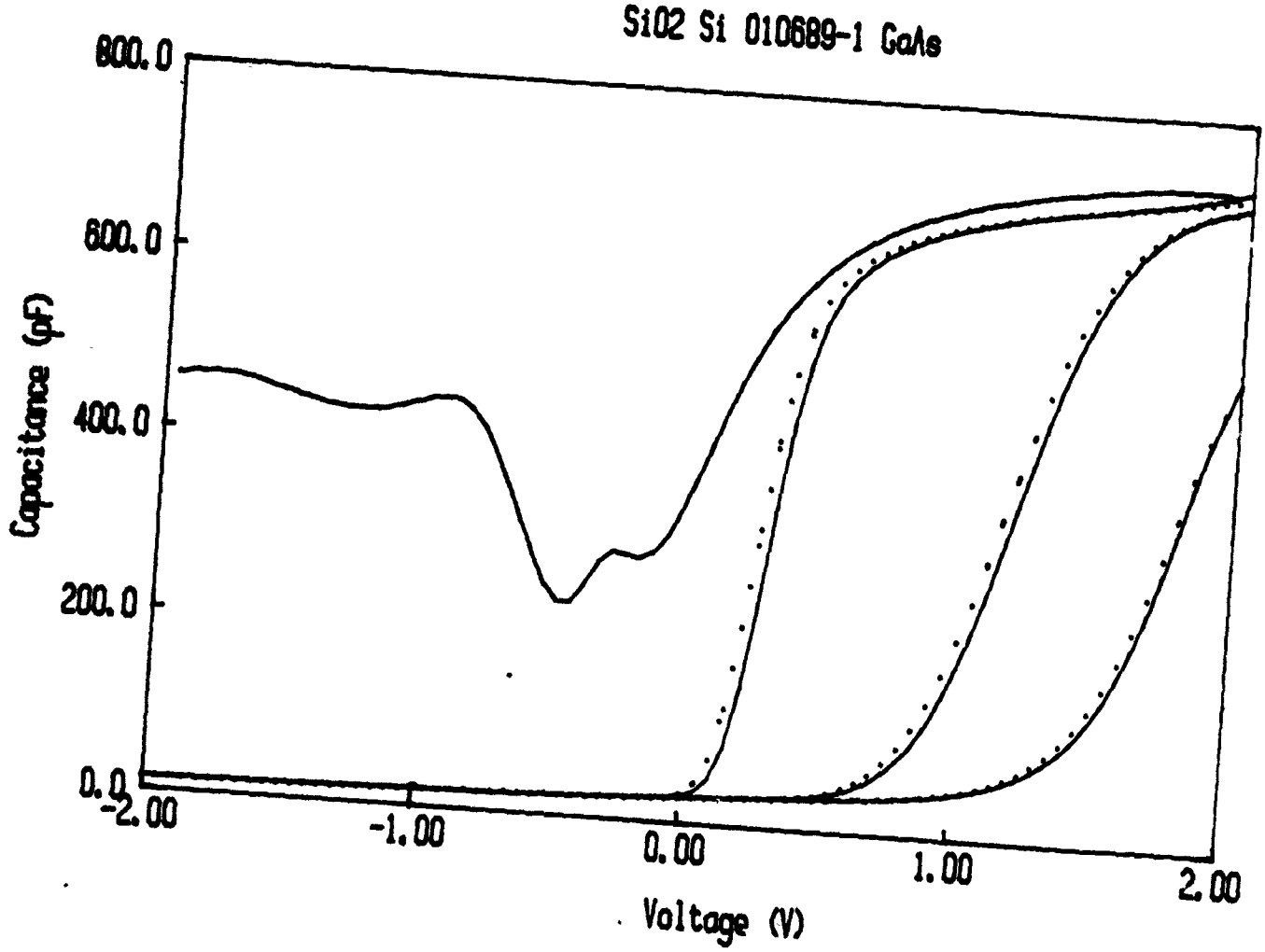


FIGURE 4.3: Multiple frequency C/V data from a n-type GaAs-pseudomorphic insulator MIS structure: The frequencies are (right to left) 10 MHz. 1 MHz. 100 KHz. quasistatic.

5.0 GaAs MIS STRUCTURES FABRICATED USING VARIOUS PROCESSING PROCEDURES

Various procedures have been implemented for the formation of the SiO_2-Si-GaAs insulator structure. These procedures have involved variation of processing temperature and process timing. In general the results indicate that procedures which minimize the time during which unintentional oxides can form on the surface of the GaAs form the structures with the best electrical characteristics.

Figure 5.1 shows the electrical characteristics of the structure reported last quarter. The devices for this structure were fabricated as follows:

1. Standard wet chemical treatment,
2. 350 ° C in situ activated hydrogen treatment,
3. RHEED analysis of the GaAs surface. (no reconstruction noted),
4. 1.5 nm Si deposition at 350 ° C,
5. Cool to 300 ° C,
6. Deposit 15 nm SiO_2.

Figure 5.2 shows electrical data from a second structure which used an activated hydrogen nitrogen in situ surface treatment. The process was carried out as follows:

1. Standard wet chemical treatment,
2. 300 ° C in situ activated hydrogen nitrogen treatment,
3. RHEED analysis of the GaAs surface. (reconstruction noted).
4. 1.5 nm Si deposition at 300 ° C.,
5. Deposit 15 nm of SiO_2.

Note that this data shows less hysteresis and less frequency dispersion than the data shown in Figure 5.1. The quasistatic data shows evidence of deep depletion

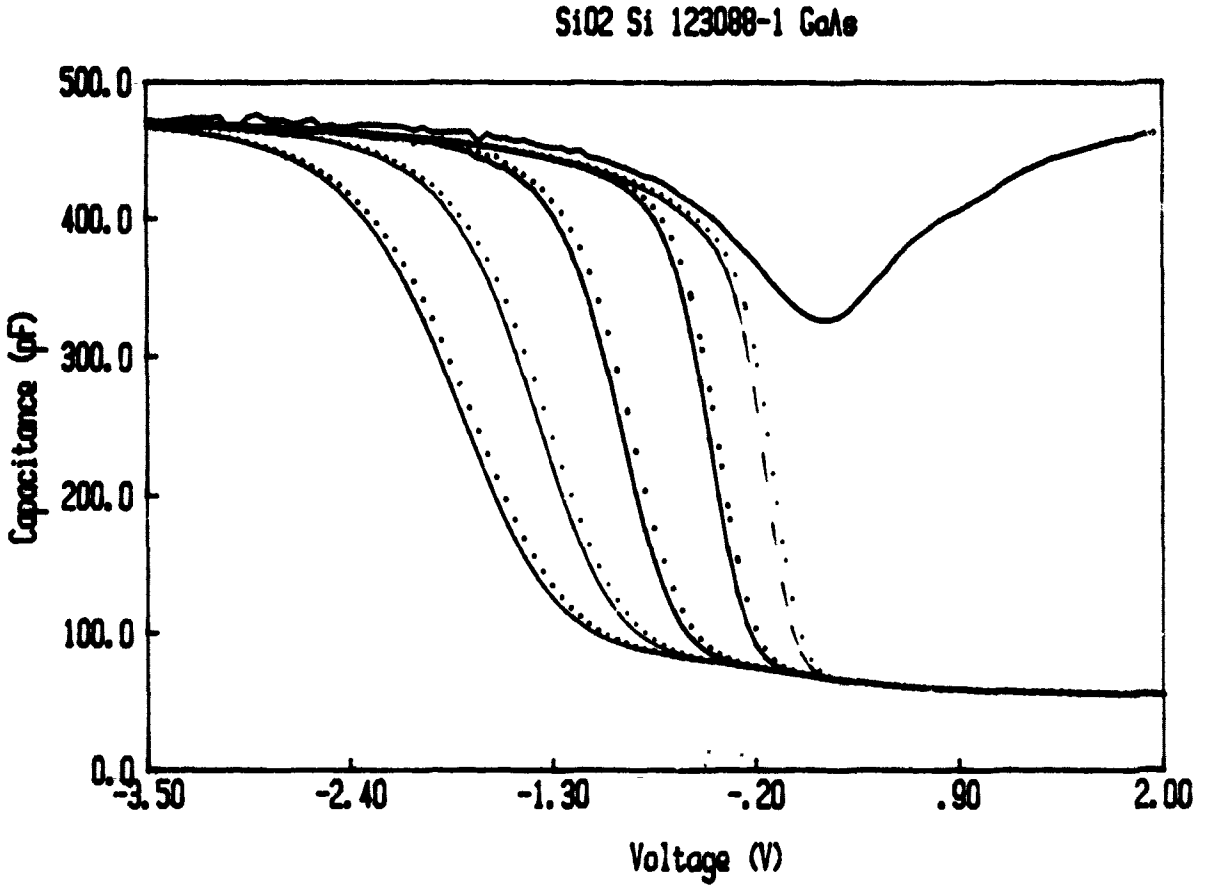


FIGURE 5.1: Multiple frequency CV data from a p-type GaAs-pseudomorphic insulator MIS structure. The processing is described in the text. The frequencies of the curves are (left to right) 10 MHz, 1 MHz, 1 MHz, 100 KHz, 10 KHz.

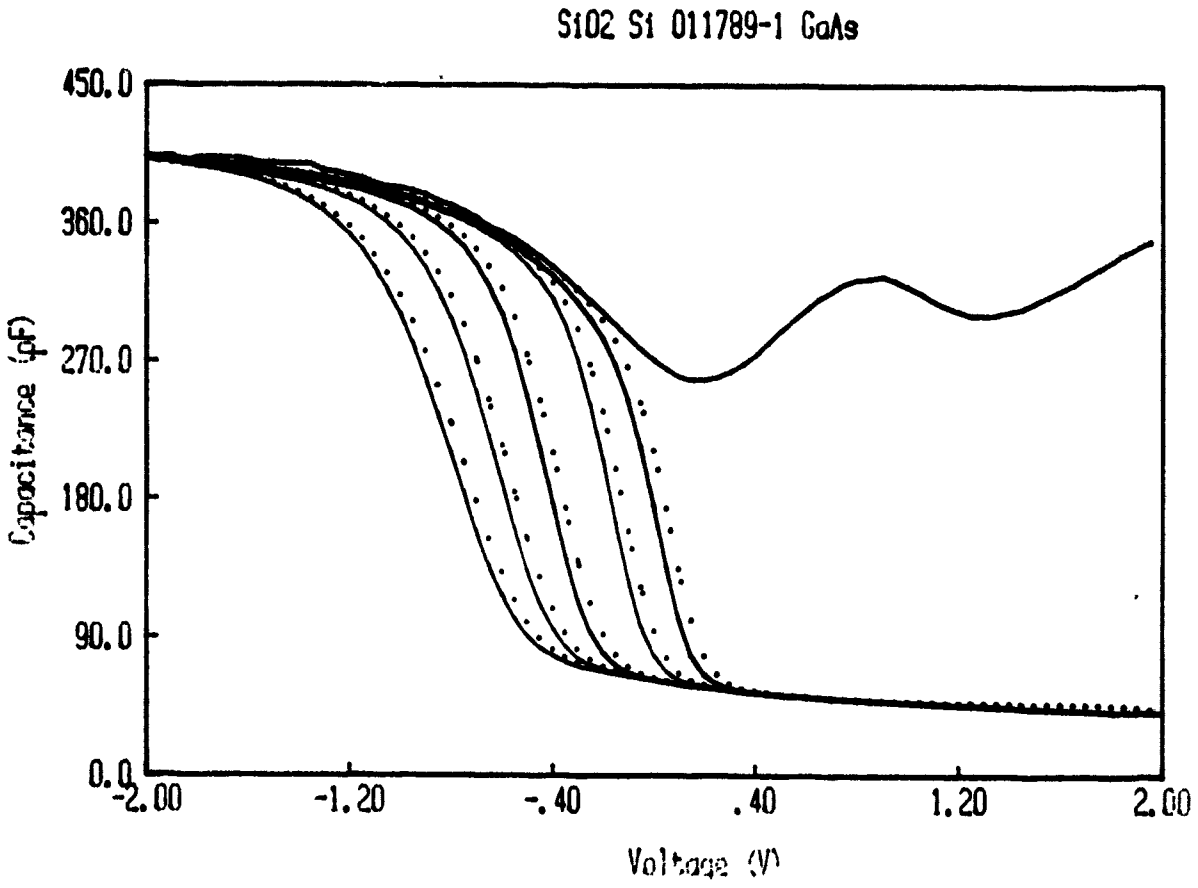


FIGURE 5.2: Multiple frequency CV data from a p-type GaAs-pseudomorphic insulator MIS structure. The processing is described in the text. The frequencies of the curves are (left to right) 10 MHz, 4 MHz, 1 MHz, 100 KHz, 10 KHz.

behavior indicating long minority lifetime.

The third sample utilized a 375 ° C in situ treatment which resulted in surface reconstruction. The processing was as follows:

1. Standard wet chemical treatment,
2. 375 ° C in situ activated hydrogen treatment,
3. RHEED analysis of the GaAs surface. (reconstruction noted),
4. 1.5 nm Si deposition at 375 ° C,
5. Cool to 300 ° C,
6. Deposit 15 nm SiO_2.

The data in Figure 5.3 shows much reduced hysteresis in the high frequency regime, in fact there is very little hysteresis at all. The frequency dispersion is also reduced from the dispersion in the data shown in Figure 5.1.

The fourth sample was processed with no stopping between the in situ clean, the Si deposition and the SiO_2 deposition. Data from this sample is shov n Figure 4. The process was carried out as follows:

1. Standard wet chemical treatment,
2. 300 ° C in situ activated hydrogen treatment,
3. 1.5 nm Si deposition at 300 ° C,
4. Deposit 15 nm SiO_2.

This sample showed much reduced dispersion in the high frequency characteristics. The hysteresis was slightly more than that shown in the data in Figure 5.3: however it is still less than that in Figure 5.1. The deep depletion behavior in the quasistatic data is significantly increased, indicating long minority carrier lifetime.

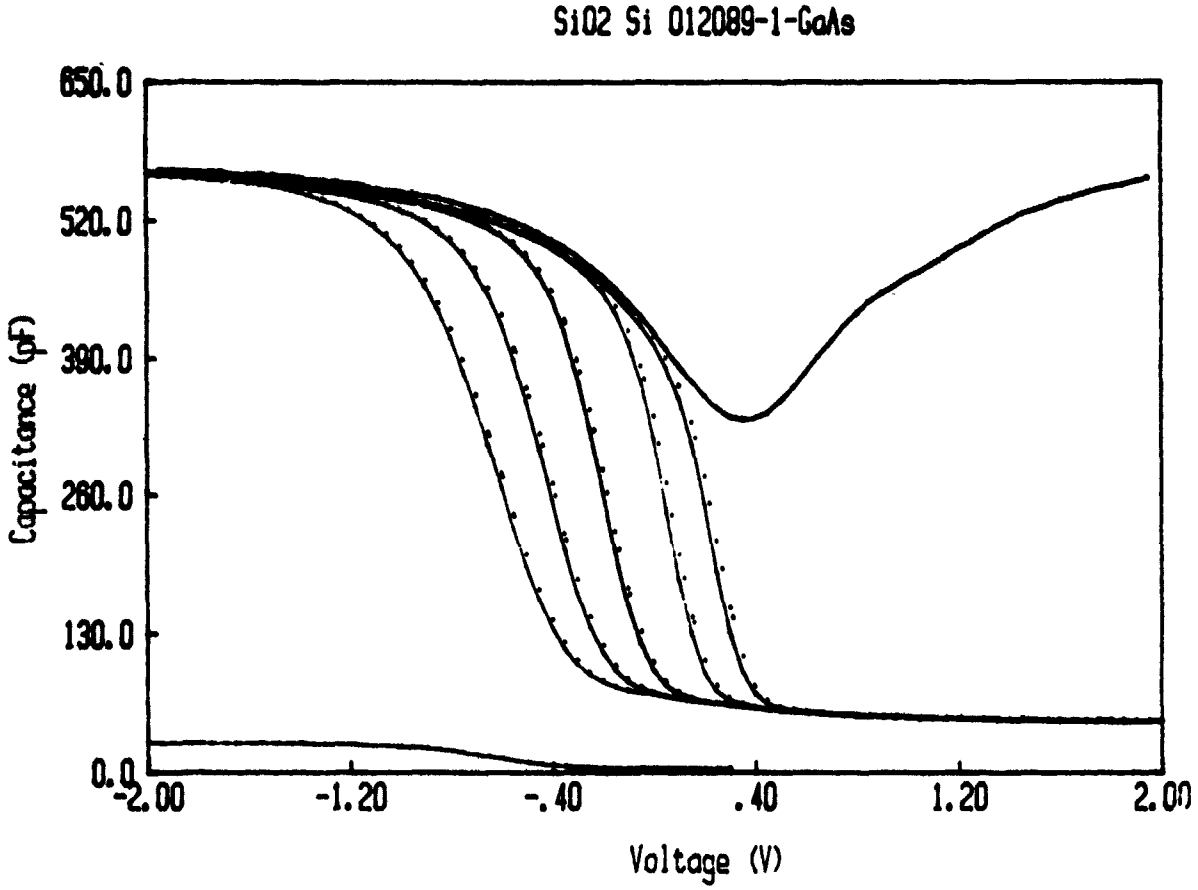


FIGURE 5.3: Multiple frequency CV data from a p-type GaAs-pseudomorphic insulator MIS structure. The processing is described in the text. The frequencies of the curves are (left to right) 10 MHz, 4 MHz, 1 MHz, 100 KHz, 10 KHz.

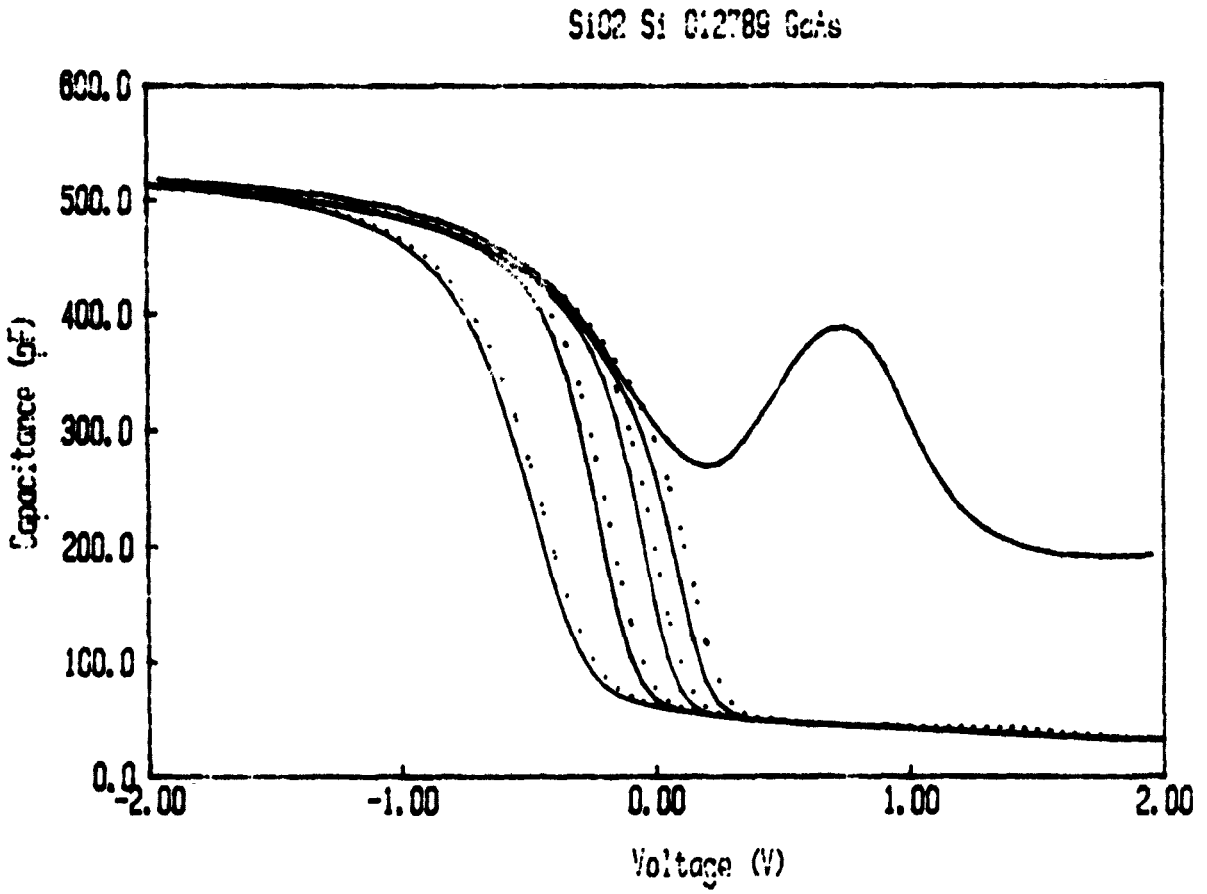


FIGURE 5.4: Multiple frequency CV data from a p-type GaAs-pseudomorphic insulator MIS structure. The processing is described in the text. The frequencies of the curves are (left to right) 10 MHz, 1 MHz, 100 KHz, 10 KHz.

As was stated earlier, it appears that processing aimed at reducing the time available for the GaAs surface to become oxidized (i.e. time during RHEED analysis or time during periods waiting for a temperature to be reduced) leads to reduced dispersion in the characteristics. Obtaining a reconstructed surface seemed to aid in the reduction of hysteresis in the high frequency data.

6.0 MASK SET FOR FET FABRICATION

A diagram of the MISFET mask set which is now in house is shown in Figure 6.1. Each die of the pattern includes GaAs MISFET structures, MIS capacitors, gate Hall measurements fixture, contact resistance pattern, and a DRAM storage cell. Thus the transistors can be fabricated and their characteristics compared with the interfacial trapping information from the capacitors, mobility information from the gated Hall structure and contact resistance information from the contact resistance test pattern.

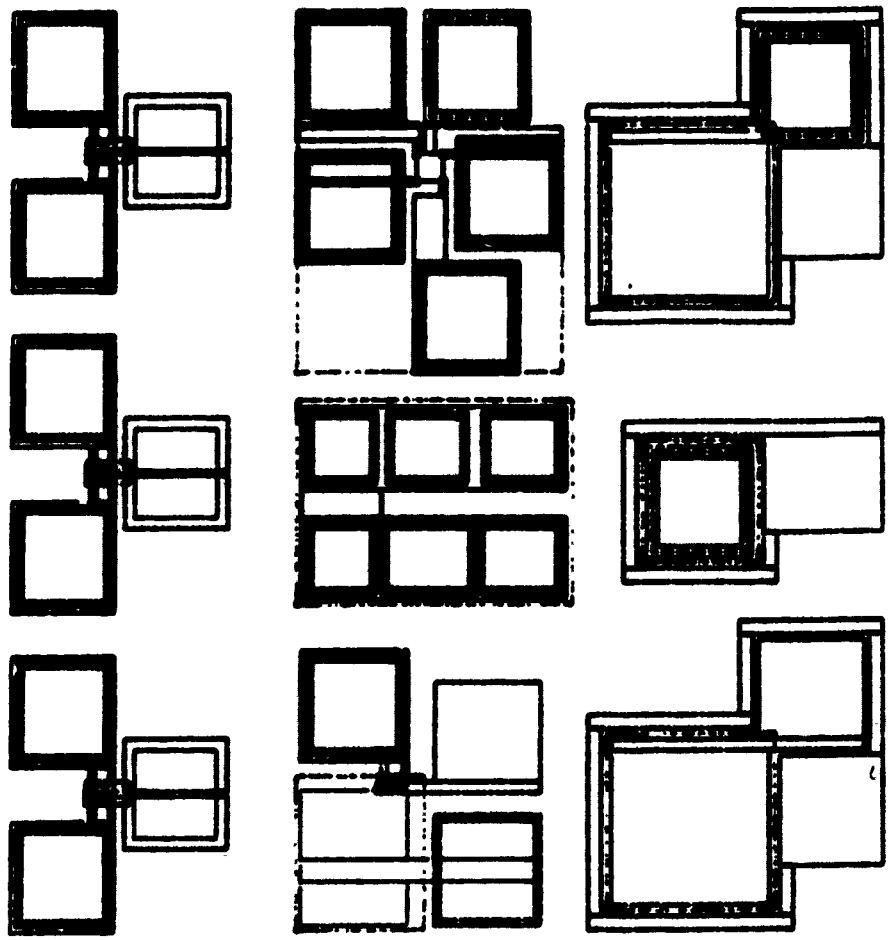


FIGURE 6.1: Diagram of the FET mask die. The FETs are on the left hand side. The gate width is 50 microns and the gate lengths are (top to bottom) 4. 3. and 2 microns. The Hall pattern is in the center top section with the contact resistance pads just below. The DRAM cell is located center bottom. The MIS capacitors are on the right hand side.

7.0 WORKSHOP PRESENTATION

A presentation was prepared and delivered at a workshop sponsored by Dr. Y. S. Park on instabilities in III-V materials and devices (April,1989 in Sedona. Arizona). The presentation discussed the in situ cleaning results, the MIS results. and the implications of these towards GaAs processing and devices.

8.0 SUMMARY AND PREVIEW

Studies to optimize the interface formation process including in situ surface cleaning and Si interlayer deposition were initiated and are in fact still proceeding. This work is of utmost importance since formation and preservation of the interface is the basis for the pseudomorphic gating technology.

Improvements have been realized in the deposition of Si at low temperature by using low pressure deposition conditions. Using these low pressure conditions pseudomorphic insulator structures have been realized using p type material and repeated (with improved results) using n type material. Capacitance-Voltage analysis indicates that both the p and n type material can be inverted as well as accumulated.

We have examined various in situ treatment techniques and their effects on the electrical characteristics of the MIS structures. Improvements have been made in the electrical performance of the devices. In particular we noted reductions in hysteresis and dispersion in the capacitance voltage characteristics of the MIS structures.

A mask set has been designed and fabricated to allow GaAs MISFET fabrication. A presentation was prepared and delivered at a workshop sponsored by Dr. Y.S. Park on instabilities in III-V materials and devices.

During the upcoming year we intend to carry out further studies of the effects on the GaAs surface chemistry of the in situ cleaning. We also plan to continue the analysis of the MIS structures including MISFET devices. A new set of issues

related to MISFET fabrication must be addressed, in particular, issues related to source drain formation.